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10/621,067	07/16/2003	Keith Farkas	200210109-1	1252

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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/621,067	FARKAS ET AL.	
	Examiner	Art Unit	
	Kenneth Tang	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-8,11,12,15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 5-8, 11-12, 15, and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the Amendment on 11/5/07. Applicant's arguments have been fully considered but were not found to be persuasive. In addition, Applicant's amendments to the claims have prompted the new grounds of rejections.

2. Claims 1-2, 5-8, 11-12, 15, and 17-24 are presented for examination.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225

USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents).

5. Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,093,147 B2 in view of Orenstien et al. (hereinafter Orenstien) (US 2003/0110012 A1).

6. As to claim 1, U.S. Patent No. 7,093,147 B2 teaches a computer system, comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and in which all execute the same instruction set (col. 8, lines 50-53); and

a performance measurement (col. 8, lines 61-63) and transfer mechanism for distributing a plurality of computer processing jobs amongst the plurality of computer processor cores (col. 8, lines 64-67).

7. U.S. Patent No. 7,093,147 B2 is silent in disclosing that the transfer mechanism is done to improve a throughput metric.

8. However, Orenstien teaches a computer system monitoring the operational activity of its dual-core processor 200 to provide load balancing between the cores by migrating processes from one core to the other based on a performance metric ([0017], [0022]-[0023]). Orenstien teaches that the performance metric, for example, can be based on power, or load for load balancing, or other things (page 2, last line of [0021]). The result of this migration based on the

monitoring of the performance measurement is an increase in throughput or clock frequency for each core ([0020], [0026], [0037], [0039]).

9. U.S. Patent No. 7,093,147 B2 and Orenstien are analogous art because they are from the same field of endeavor of selecting processor cores and in the same problem solving area of improving overall system efficiency.

10. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify U.S. Patent No. 7,093,147 B2 to include Orenstein's features of migrating processes to cores to improve a throughput metric.

11. The suggestion/motivation for doing so would have been to improve the performance of the system. An improved throughput metric results in an improved performance of the system.

12. Claim 7 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 7,093,147 B2 in view of Orenstien et al. (hereinafter Orenstien) (US 2003/0110012 A1).

13. As to claim 7, U.S. Patent No. 7,093,147 B2 teaches a method for operating multiple processor cores, comprising:

placing a plurality of computer processor cores on a single semiconductor die, in which at least two computer processor cores differ in processing performance, and in which all execute the same instruction set (col. 10, lines 39-46);

measuring the performance of each of a plurality of computer processing jobs hosted amongst the plurality of computer processor cores (col. 10, lines 49-51); and

transferring individual ones of said plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (col. 10, lines 52-55).

14. U.S. Patent No. 7,093,147 B2 is silent in disclosing that the transfer mechanism is done to improve a throughput metric.

15. However, Orenstien teaches a computer system monitoring the operational activity of its dual-core processor 200 to provide load balancing between the cores by migrating processes from one core to the other based on a performance metric ([0017], [0022]-[0023]). Orenstien teaches that the performance metric, for example, can be based on power, or load for load balancing, or other things (page 2, last line of [0021]). The result of this migration based on the monitoring of the performance measurement is an increase in throughput or clock frequency for each core ([0020], [0026], [0037], [0039]).

16. U.S. Patent No. 7,093,147 B2 and Orenstien are analogous art because they are from the same field of endeavor of selecting processor cores and in the same problem solving area of improving overall system efficiency.

17. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify U.S. Patent No. 7,093,147 B2 to include Orenstein's features of migrating processes to cores to improve a throughput metric.

18. The suggestion/motivation for doing so would have been to improve the performance of the system. An improved throughput metric results in an improved performance of the system.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

19. Claims 1, 2, 5-8, 11-12, 15, 17, 19, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Orenstien et al. (hereinafter Orenstien) (US 2003/0110012 A1).

20. As to claim 1, Orenstien teaches a computer system, comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and in which all execute the same instruction set ([0017], [0022]-[0023]); and

a performance measurement (power consumption metric or alternatively, a load measurement that is used to in the load balancing between the processor cores) (page 2, last line of [0021]) and transfer mechanism for distributing a plurality of computer processing jobs amongst the plurality of computer processor cores to improve a throughput metric (tracking and migration of processes from one core to the other in a dual core processor 200 to increase throughput, clock frequency, the amount of processing, etc.) ([0020], [0026], [0037], [0039]).

21. In summary of the above citations, Orenstien teaches a computer system monitoring the operational activity of its dual-core processor 200 to provide load balancing between the cores by migrating processes from one core to the other based on a performance metric. Orenstien teaches that the performance metric, for example, can be based on power, or load for load balancing, or other things. The result of this migration based on the monitoring of the performance measurement is an increase in throughput or clock frequency for each core.

22. As to claim 2, Orenstien teaches further comprising: at least one of an operating system (operating system 755, [0041]-[0042]), hosted on the plurality of computer processor cores, firmware ([0026]), and special-purpose hardware that includes the performance measurement and transfer mechanism (monitor 110, [0020]-[0021]), and that provides for a periodic test to determine relative performance of different jobs on different ones of the plurality of computer processor cores (relative performance of each core is periodically monitored and evaluated such that the load can be leveled or balanced) ([0021], [0027]).

23. As to claim 5, Orenstien teaches further comprising: at least one of an operating system hosted on the plurality of computer processor cores (operating system 755, [0041]-[0042]), firmware ([0026]), and special-purpose hardware that includes the performance measurement and transfer mechanism (monitor 110, [0020]-[0021]), and that provides for a periodic test of operating states within each of the computer processor cores in making a decision as to where to place a given processing software workload (relative performance of each core is periodically monitored and evaluated such that the load can be leveled or balanced) ([0021]), wherein said operating states are dependent on at least one of the operating voltage and clock frequency of a corresponding one of the plurality of computer processor cores ([0033]-[0034], [0037]).

24. As to claim 6, Orenstien teaches further comprising: at least one of an operating system hosted on the plurality of computer processor cores (operating system 755, [0041]-[0042]), firmware ([0026]), and special-purpose hardware that includes the performance measurement and transfer mechanism (monitor 110, [0020]-[0021]), and that provides for a periodic test of operating states within each of the computer processor cores in a making decision as to where to place a given processing software workload (relative performance of each core is periodically monitored and evaluated such that the load can be leveled or balanced) ([0021]), wherein said operating states are dependent on run-time re-configuration of hardware structures of corresponding ones of the plurality of computer processor cores ([0018], [0020]).

25. As to claim 7, Orenstien teaches a method for operating multiple processor cores, comprising:

placing a plurality of computer processor cores on a single semiconductor die, in which at least two computer processor cores differ in processing performance, and in which all execute the same instruction set ([0022]-[0023], [0017]);

measuring the performance of each of a plurality of computer processing jobs hosted amongst the plurality of computer processor cores ([0019]); and

transferring individual ones of said plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (tracking and migration of processes from one core to the other in a dual core processor 200 to increase throughput, clock frequency, the amount of processing, etc.) ([0020]-[0021], [0027]).

26. In summary of the above citations, Orenstien teaches a computer system monitoring the operational activity of its dual-core processor 200 to provide load balancing between the cores by migrating processes from one core to the other based on a performance metric. Orenstien teaches that the performance metric, for example, can be based on power, or load for load balancing, or other things. The result of this migration based on the monitoring of the performance measurement is an increase in throughput or clock frequency for each core.

27. As to claim 8, Orenstien teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (relative

performance of each core is periodically monitored and evaluated such that the load can be leveled or balanced) ([0021], [0027]).

28. As to claim 11, it is rejected for the same reasons as stated in the rejection of claim 5.

29. As to claim 12, it is rejected for the same reasons as stated in the rejection of claim 6.

30. As to claim 15, Orenstien teaches further comprising: associating workloads for execution on specific processor cores based on at least one of user and application hints ([0042]).

31. As to claim 17, Orenstien teaches further comprising at least one of an operating system hosted on the plurality of computer processor cores (multi-core), firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism ([0041], [0026]).

32. As to claim 19, Orenstien teaches wherein the performance measurement and transfer mechanism periodically transfers the executing computer processing jobs to a new assignment amongst the plurality of computer processor cores, collects performance statistics about execution at the new assignment, and then determines whether to reassign the executing

computer processing jobs to different computer processor cores based on the performance statistics collected (relative performance of each core is periodically monitored and evaluated such that the load can be leveled or balanced via process migration between cores) ([0021], [0027]).

33. As to claim 22, Orenstien teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics (information can be provided by user, the program itself, or the execution of the program) ([0042]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claims 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orenstien et al. (hereinafter Orenstien) (US 2003/0110012 A1) in view of Schmeck et al. (hereinafter Schmeck) ("Trends in Network and Pervasive Computing – ARCS 2002", April 2002).

35. As to claim 18, Orenstien teaches wherein the performance measurement and transfer mechanism improves the total system throughput. Orenstien is silent wherein the throughput is maximized. However, Schmeck teaches that a single processor containing multiple clusters can be optimized and that the goal is to maximize the total number of instructions per second (throughput) (see page 157 under Section 3.5: Optimization). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Orenstien such that the total system throughput is maximized because it would provide the predicted result of improved performance of the system.

36. As to claim 23, Orenstien is silent wherein the throughput metric comprises a number of instructions per second. However, Orenstien does teach improving a throughput metric such as clock frequency of the processor. In addition, Schmeck teaches a single processor containing multiple clusters that can be optimized by maximizing the total number of instructions per second (see page 157 under Section 3.5: Optimization). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Orenstien such that the throughput metric would comprise of a number of instructions per second. The suggestion/motivation for doing so would have been to provide the predicted result of having a metric that can be used to optimize and maximize the system (see page 157 under Section 3.5: Optimization).

37. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orenstien et al. (hereinafter Orenstien) (US 2003/0110012 A1) in view of Matoba (US 5,913,068).

38. As to claim 20, Orenstien teaches wherein the performance measurement and transfer mechanism swaps execution of the executing computer processing jobs between the computer processor cores for a period of time, and monitoring resulting and relative performance of the cores (relative performance of each core is periodically monitored and evaluated such that the load can be leveled or balanced) ([0021], [0027]). Orenstien is silent in building a table to contain the information of the relative performance of jobs on different types of cores. However, Matoba teaches switching CPUs based on load state of each CPU and having a process management table 23 that collects and manages the information regarding the allocation (col. 7, lines 56-67, col. 8, lines 31-42, col. 9, lines 4-19). Orenstien and Matoba are analogous art because they both are related to power saving in a parallel processing environment. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Orenstien such that it would include a table to manage and organize the information related to the monitoring functions and performance results. The suggestion/motivation for doing so would have been to provide the predicted result of improving the management and organization of data.

39. As to claim 21, Orenstien teaches wherein the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex processor cores to said large complex processor cores (the monitor value may be a simple or complex activity factor that reflects the operational activity of a particular processing unit; migration is done based on monitor value) ([0019]).

40. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Orenstien et al. (hereinafter Orenstien) (US 2003/0110012 A1) in view of Diepstraten et al. (hereinafter Diepstraten) (US 6,986,141 B1).

41. As to claim 24, Orenstien is silent wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals. However, Diepstraten teaches having time slice task switching capability in its switching or processes (col. 1, lines 52-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Orenstien's migration of proceses to include the feature of wherein the movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals. The suggestion/motivation for doing so would have been to provide the predicted result of a more flexible way to allocate and manage context (col. 3, lines 44-67).

Response to Arguments

42. Applicant argues on page 10 of the Remarks that the obvious-type double patenting rejections of claims 1 and 7 should be withdrawn due to the amendment of those claims indicating that the computer processor cores improve a throughput metric.

43. Applicant's amendment necessitated the new ground of rejection regarding obvious-type double patenting with U.S. Patent No. 7,093,147 in view of Orenstien (US 2003/0110012 A1). Therefore, the double patenting rejections of claims 1 and 7 have not been withdrawn.

44. The Examiner has withdrawn the double patenting rejection based on claim 16 in response to the Applicant cancelling that claim.

45. Applicant argues, on pages 11-12, that the claim amendment reciting "to improve a throughput metric" is not found in Orenstien.

46. In response, Orenstien teaches a computer system monitoring the operational activity of its dual-core processor 200 to provide load balancing between the cores by migrating processes from one core to the other based on a performance metric ([0017], [0022]-[0023]). Orenstien teaches that the performance metric, for example, can be based on power, or load for load balancing, or other things (page 2, last line of [0021]). The result of this migration based on the

monitoring of the performance measurement is an increase in throughput or clock frequency for each core ([0020], [0026], [0037], [0039]). Thus, Orenstien does teach the amended limitation, and therefore, the rejections based on 35 U.S.C. 102 for claims 1 and 7 have been maintained.

47. Applicant has added new claims 17-24. In response to the newly added claims, rejections have been made as claims 17-24 were not found to contain any allowable subject matter.

Conclusion

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Hong et al. ("Power Optimization of Variable-Voltage Core-Based Systems", December 1999) discloses optimization of a multli-core processor by resource allocation and power (see Abstract).**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kt
1/12/08

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